We claim:

1. A microprocessor for processing various assembler codes, comprising:

a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place; and

a plurality of program counters and, dependent on the parameter, in each case one of said program counters is active in a computation of relative addresses.

2. The microprocessor according to claim 1, including:

a computation unit; and

a multiplexer connected to said program counters, said multiplexer receives and is controlled by the parameter, said multiplexer having an output connected to said computation unit for the relative addresses.

3. A microprocessor for processing various assembler codes, comprising:

a multiplexer having a first input, a second input for receiving a 0 value, and a third input receiving a parameter

designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place;

a program counter;

a computation unit for computing relative addresses;

an adding unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a second input connected to said multiplexer, and an output connected to said computation unit; and

a memory for storing an instruction length and having an output connected to said first input of said multiplexer.

4. A microprocessor for processing various assembler codes, comprising:

a multiplexer having a first input, a second input for receiving a 0 value, and a third input receiving a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place;

a program counter;

a computation unit for computing relative addresses;

an subtracting unit connected between said program counter and said computation unit for the relative addresses, said subtracting unit having a first input connected to said program counter, a second input connected to said multiplexer, and an output connected to said computation unit; and

a memory for storing an instruction length and having an output connected to said first input of said multiplexer.

5. A method of relative addressing in a microprocessor, which comprises the steps of:

determining relative addresses in dependence on one of an operating state and a parameter for a respective assembler code;

providing a plurality of program counters for various operating states and assembler codes; and

selecting one of the program counters for use in determining the relative addresses in dependence on one of the operating state and the respective assembler code.

6. The method according to claim 5, which comprises performing one of:

performing one of an addition and a subtraction of an instruction length to/from a program counter reading for a relative address computation in dependence on one of the various operating states and the assembler codes; and

leaving the program counter reading unchanged.

7. The method according to claim 6, which comprises performing one of:

performing one of an addition and a subtraction of the instruction length to/from an offset value used for the computation of the relative addresses in dependence on one of the various operating states and the assembler codes; and

leaving the offset value unchanged.